

## NCE N-Channel Enhancement Mode Power MOSFET

### Description

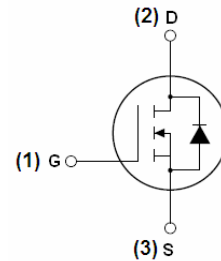
The NCE0130G uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

### General Features

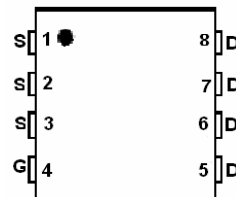
- $V_{DS} = 100V, I_D = 30A$   
 $R_{DS(ON)} < 28m\Omega @ V_{GS}=10V$  (Typ:24m $\Omega$ )
- Special process technology for high ESD capability
- High density cell design for ultra low  $R_{dson}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation

### Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



Schematic diagram



Marking and pin assignment



DFN5X6-8L top view

### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE0130G	NCE0130G	DFN5X6-8L	-	-	-

### Absolute Maximum Ratings ( $T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Limit	Unit
$V_{DS}$	Drain-Source Voltage	100	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current-Continuous	30	A
$I_D(100^\circ C)$	Drain Current-Continuous( $T_C=100^\circ C$ )	21	A
$I_{DM}$	Pulsed Drain Current	70	A
$P_D$	Maximum Power Dissipation	75	W
	Derating factor	0.5	W/ $^\circ C$
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	-55 To 175	$^\circ C$

### Thermal Characteristic

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	2.0	$^\circ C/W$
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**Electrical Characteristics ( $T_C=25^{\circ}\text{C}$  unless otherwise noted)**

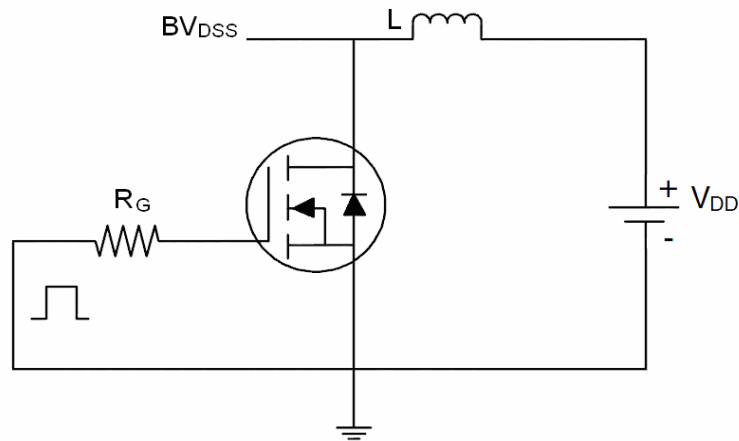
Symbol	Parameter	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	100	110	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=100V, V_{GS}=0V$	-	-	1	$\mu A$
$I_{GSS}$	Gate-Body Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics (Note 3)</b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3	4	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	$V_{GS}=10V, I_D=10A$	-	24	28	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS}=5V, I_D=10A$	-	15	-	S
<b>Dynamic Characteristics (Note 4)</b>						
$C_{iss}$	Input Capacitance	$V_{DS}=25V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	2000	-	PF
$C_{oss}$	Output Capacitance		-	300	-	PF
$C_{rss}$	Reverse Transfer Capacitance		-	250	-	PF
<b>Switching Characteristics (Note 4)</b>						
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=50V, R_L=5\Omega$ $V_{GS}=10V, R_{GEN}=3\Omega$	-	7	-	nS
$t_r$	Turn-on Rise Time		-	7	-	nS
$t_{d(off)}$	Turn-Off Delay Time		-	29	-	nS
$t_f$	Turn-Off Fall Time		-	7	-	nS
$Q_g$	Total Gate Charge	$V_{DS}=50V, I_D=18A,$ $V_{GS}=10V$	-	39	-	nC
$Q_{gs}$	Gate-Source Charge		-	8	-	nC
$Q_{gd}$	Gate-Drain Charge		-	12	-	nC
<b>Drain-Source Diode Characteristics</b>						
$V_{SD}$	Diode Forward Voltage (Note 3)	$V_{GS}=0V, I_S=20A$	-	-	1.2	V
$I_S$	Diode Forward Current (Note 2)	-	-	-	30	A
$t_{rr}$	Reverse Recovery Time	$T_J = 25^{\circ}\text{C}, I_F = 18A$ $di/dt = 100A/\mu s$ (Note 3)	-	32	-	nS
$Q_{rr}$	Reverse Recovery Charge		-	53	-	nC
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Notes:**

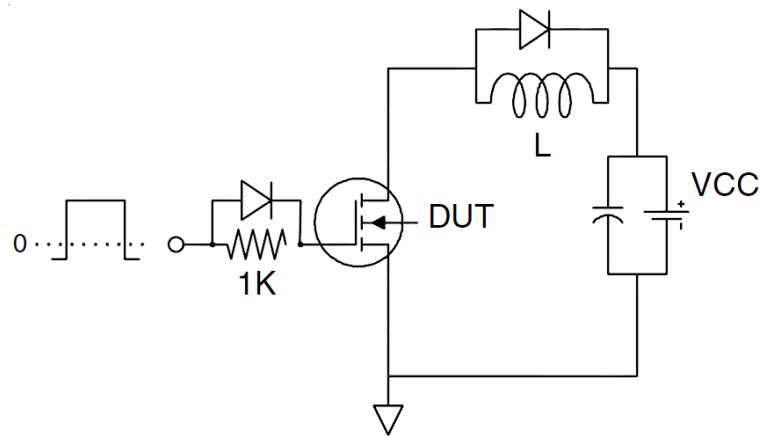
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production

**Test Circuit**

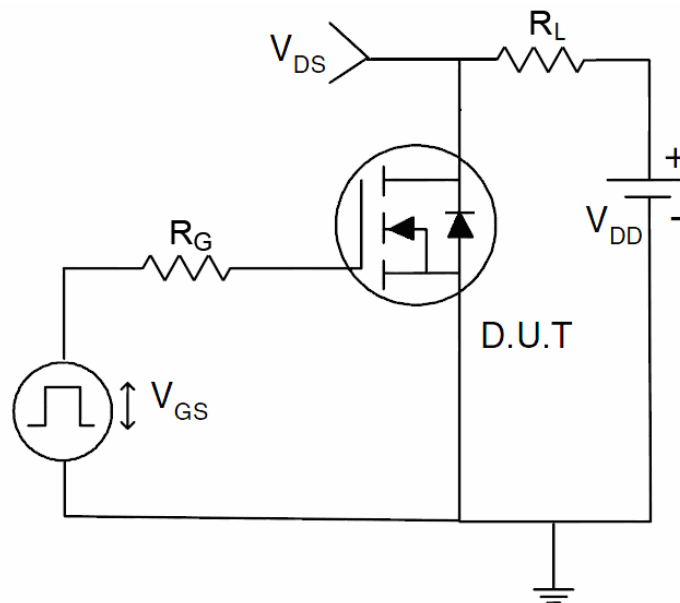
**1) E<sub>AS</sub> Test Circuit**



**2) Gate Charge Test Circuit**



**3) Switch Time Test Circuit**



Typical Electrical and Thermal Characteristics (Curves)

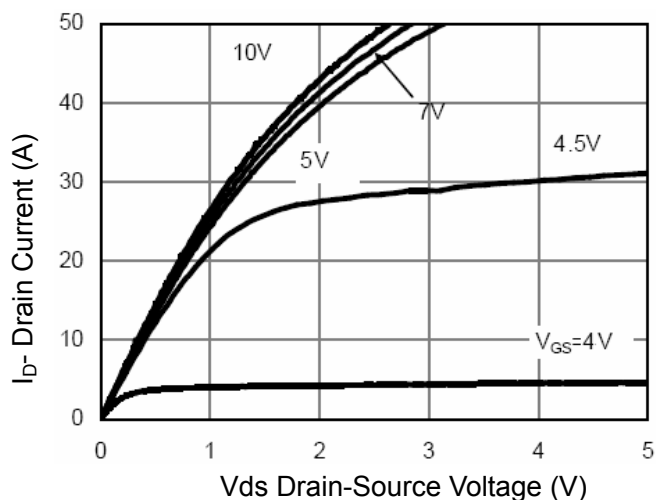


Figure 1 Output Characteristics

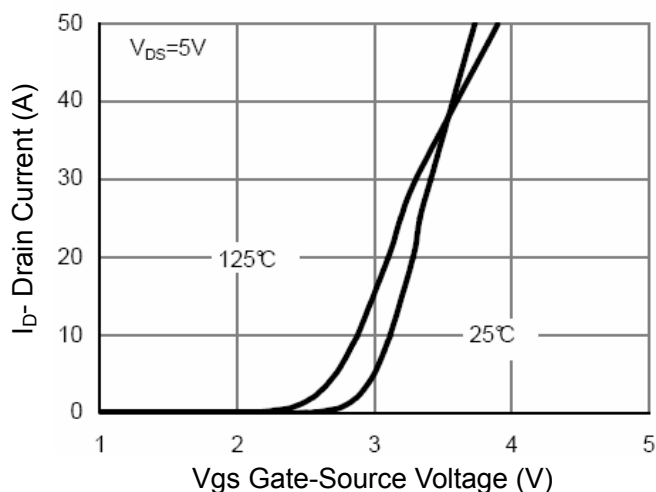


Figure 2 Transfer Characteristics

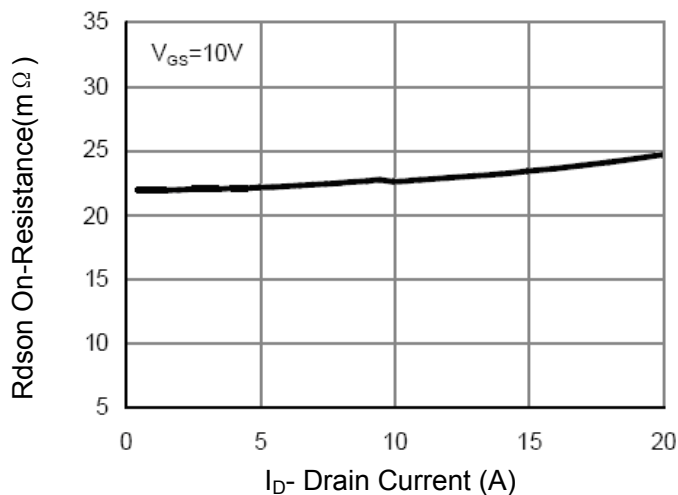


Figure 3 Rdson- Drain Current

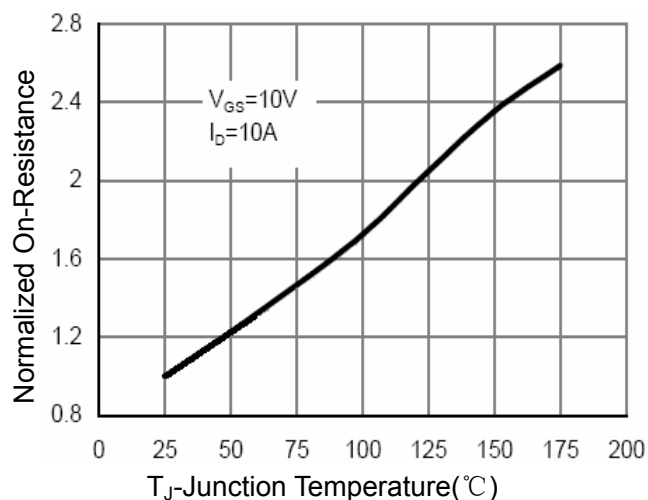


Figure 4 Rdson-Junction Temperature

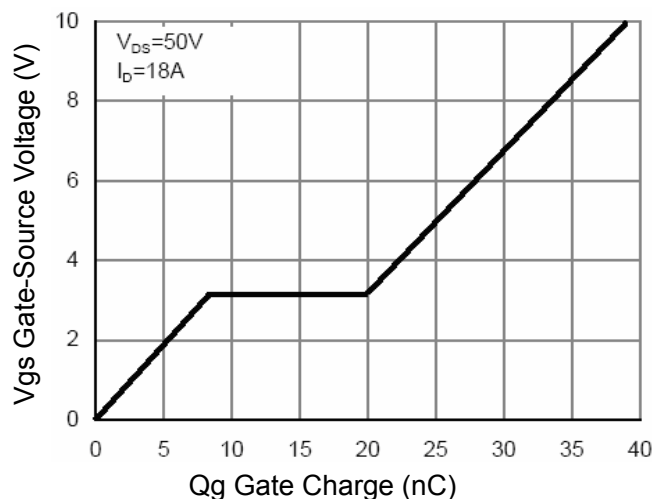


Figure 5 Gate Charge

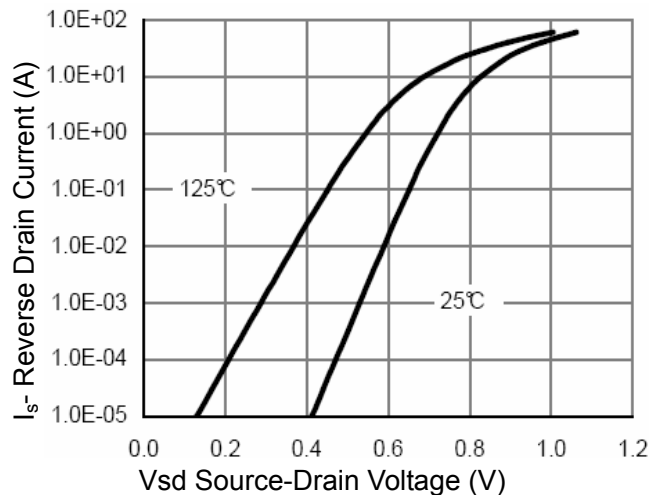


Figure 6 Source- Drain Diode Forward

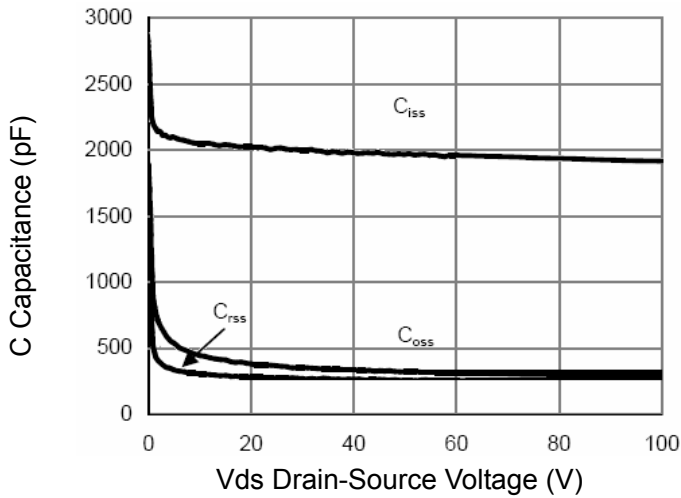


Figure 7 Capacitance vs Vds

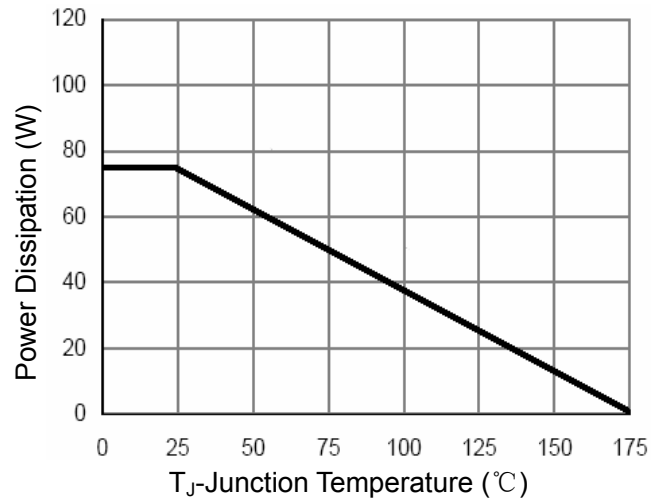


Figure 9 Power De-rating

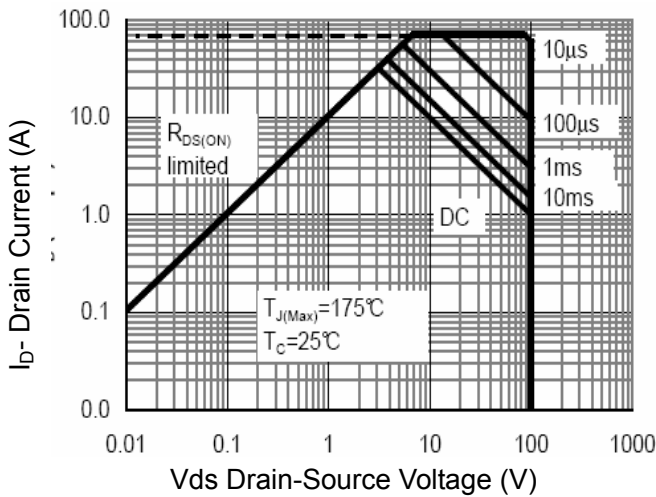


Figure 8 Safe Operation Area

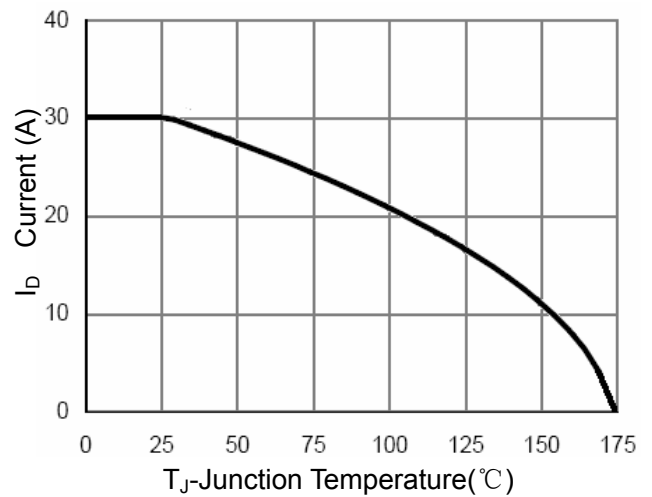


Figure 10 ID Current- Junction Temperature

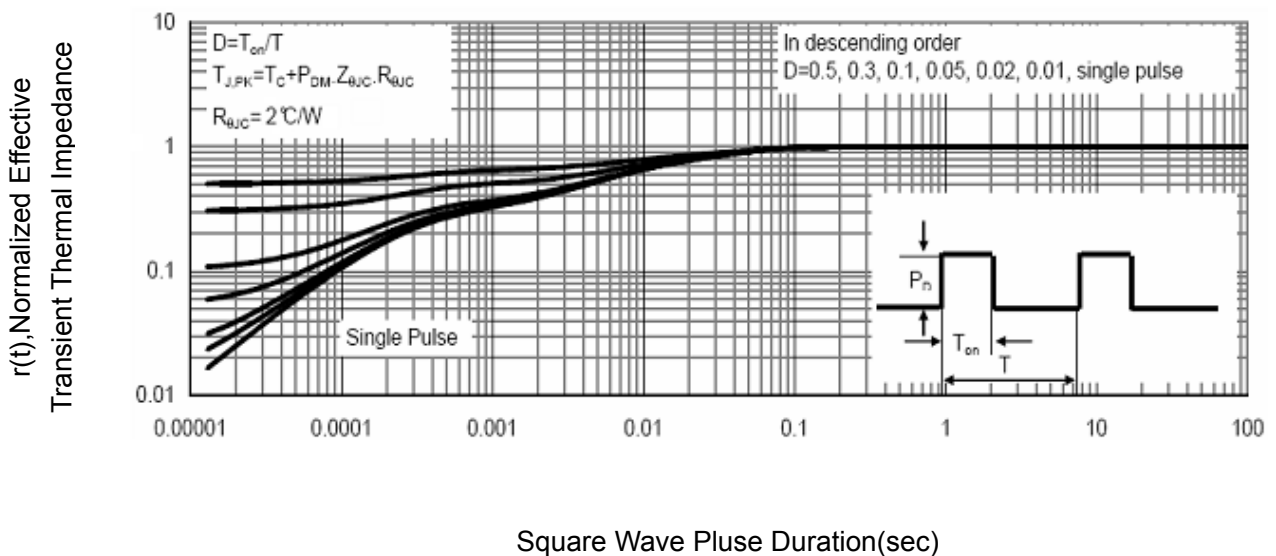
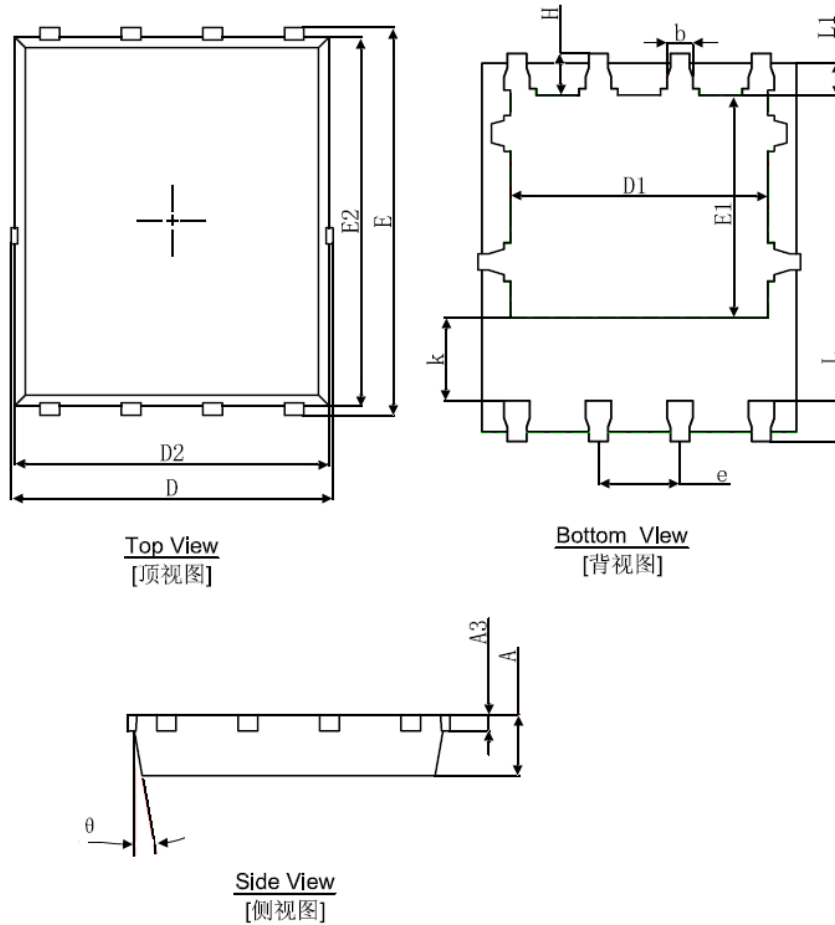


Figure 11 Normalized Maximum Transient Thermal Impedance

**DFN5X6-8L Package Information**


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
K	1.190	1.390	0.047	0.055
b	0.035	0.450	0.014	0.018
e	1.270(TYP.)		0.050(TYP.)	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
$\theta$	8°	12°	8°	12°

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